SPECIFICATION

Please replace the paragraph beginning at page 10, line 16, with the following amended paragraph:

Shown in FIG. 3 is a detailed block diagram of shifter/combiner 58, which comprises logic ~~60~~ 91 and two-input multiplexers 92, 94, 96, 98, 100, 102, 104, 106, 108, 110, 112, 114, and 116 and operate in the same way as multiplexers 80-90 shown in FIG. 2. Shifter/combiner 58 receives intermediate signals I0-I3 as described with regard to FIG. 2 and also intermediate signals I4-I7 from arranger 44 that are generated in the same manner as intermediate signals I0-I3. Multiplexer 92 has an input for receiving signal I3, and input for receiving signal I4, and an output. Multiplexer 92 has an input for receiving signal I3, an input for receiving signal I4, and an output. Multiplexer 92 has an input for receiving signal I4, an input for receiving signal I5, and an output. Multiplexer 96 has an input for receiving signal I5, an input for receiving signal I6, and an output. Multiplexer 98 has an input for receiving signal I6, an input for receiving signal I7, and an output for providing shifter/combiner signal SC6. Multiplexer 100 has an input for receiving signal I1, an input coupled to the output of multiplexer 92, and an output. . Multiplexer 102 has an input for receiving signal I2, an input coupled to the output of multiplexer 94, and an output. Multiplexer 104 has an input coupled to the output of multiplexer 92, an input coupled to the output of multiplexer 96, and an output. Multiplexer 106 has an input coupled to the output of multiplexer 94, an input coupled to the output of multiplexer 98, and an output for providing shifter/combiner signal SC4. Multiplexer 108 has an input coupled to the output of multiplexer 96, an input for receiving signal I7, and an output for providing shifter/combiner signal SC5. Multiplexer 110 has an input for receiving signal I0, an input coupled to the output of multiplexer 106, and an output for providing shifter/combiner signal SC0. Multiplexer 112 has an input coupled to the output of multiplexer 100, an input coupled to the output of multiplexer 108, and an output for providing shifter/combiner signal SC1. Multiplexer 114 has an input coupled to the output of multiplexer 102, an input coupled to the output of multiplexer 98, and an output for providing shifter/combiner signal SC2. Multiplexer 116 has an input coupled to the output of multiplexer 104, an input for receiving signal SC7, and an output for providing shifter/combiner signal SC3. Signal I7 is passed as shifter/combiner signal SC7.

Please replace the paragraph beginning at page 1, line 22, with the following amended paragraph:

Logic ~~60~~ 91 converts mask signals M0-M3 to shift control signals C1, C2, C3, and C4. Although arranger 42 does not use mask signal M3, logic ~~60~~ 91 does. Signals C1-C4 provide the information as to the amount of shift that is to occur. The information and the circuit of shift/combiner 58 allow for a shift of anywhere from zero to seven. Mask signals provide the information as to how many of the four possible bits are non-transfer bits. The logic thus provides shift control signals in the logic states that represents how many non-transfer bits were in the left most subset of the pair of subsets. In this case, the relevant subset is subset 26. The maximum number that can be non-transfer bits is four so the actual maximum shift is four. Multiplexers 92-98 each have their control input for receiving shifter control signal C1. Multiplexers 102-108 each have their control input for receiving shifter control signal C2. Multiplexer 100 has its control input for receiving shifter control signal C3. Multiplexers 110-116 each have their control input for receiving shifter control signal C4. When signals C1-C4 are all active, that means no shift. When signal C1 is inactive, there is a shift of 1. When signal C2 is inactive, there is a shift of 2. When signal C3 is active, there is a shift of three. When signal C4 is inactive, there is a shift of four. When C2 and C1 are inactive there is a shift of three. Thus, there is available a shift of zero to four. The cases for 5-7 are also available but are not necessary. Shifter/combiners 58-64 are all constructed in the same way.